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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,371	09/25/2003	In Duk Song	0465-I880PUS1	3363

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EXAMINER	
NGUYEN, LAUREN	

ART UNIT	PAPER NUMBER
2871	

NOTIFICATION DATE	DELIVERY MODE
08/30/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/669,371	SONG, IN DUK	
	Examiner	Art Unit	
	LAUREN NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,5-9 and 12-23* is/are pending in the application.

5a) Of the above claim(s) *7-9,17 and 18* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1, 5, 6, 12-16, 19-23* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed 01/14/2011 has been entered.

Response to Amendment

2. Applicant's arguments filed 01/14/2011 have been fully considered but they are not persuasive.

3. The applicant argues (see pages 11-12) Kawaguchi fails to disclose the gate control signals are directly received from the data PCB through the first TCP without the gate PCB. This is irrelevant and not persuasive. The claimed invention does not require the gate control signals to be directly received from the data PCB through the first TCP without the gate PCB. However, the applicant is alleging patentability due to a feature that is not claimed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. The applicant also argues (see pages 12-13) that Song teaches away from being properly combined with the Kawaguchi reference because it deals with applying a voltage to a storage capacitor and to a counter electrode on an upper substrate by connecting one of the storage capacitor electrodes with the counter electrode. This is also irrelevant and not persuasive. **awaguchi** (figure 1A) discloses a line-on glass liquid crystal display panel as claimed in claimed 19

but is silent regarding the silver dot. The examiner merely relies on **Song et al.** (in at least paragraph 0014, figure 4) for the teaching of at least one of the plurality of common voltage lines applies the common voltage signal through a silver(Ag) dot (63) to a common electrode that is formed on an entire surface of an upper substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the silver dot as taught by **Song et al.** because such modification would provide an electrical connection with the common electrode of the upper substrate

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 5-6, 12-16 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kawaguchi (US 6,052,171)** in view of **Yuda et al. (US 2002/0180686)**; further in view of **Kim et al. (KR 10-1999-0024956)**.

7. Regarding **claim 1**, **Kawaguchi** (figure 1A) discloses a line-on glass liquid crystal display panel, comprising:

- a picture display part having liquid crystal cells at each intersection of first ~ n(th) gate lines and first ~ n(th) data lines (see at least column 4, lines 10-20);
- **Kawaguchi** (figure 1A) implicitly discloses first ~ n(th) data pads extended from the first ~ n(th) data lines in an outer area of the picture display part; first ~ n(th) gate pads extended from the first ~ n(th) gate lines in the outer area of the picture display part; a plurality of

first line-on glass signal pads formed just beside the first gate pads and a plurality of second line-on glass signal pads formed just beside the first gate pads; the first and second line-on glass signal pads are on respective intersecting sides which define one comer of the outer area of the picture display part;

- a plurality of line-on glass type signal lines (13; see at least column 6, lines 60-65) connecting the first and second line-on glass signal pads in the comer of the outer area of the picture display part for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part; and
- **Kawaguchi** (figure 1A) implicitly discloses a plurality of first dummy pads between the first line-on glass type signal pads and a plurality of second dummy pads between the second line-on glass type signal pads; and
- a plurality of dummy lines (12) connecting the first and second dummy pads in the one corner of the outer area of the picture display part, wherein the plurality of dummy lines are formed between the line-on glass type signal lines for applying a common voltage as a reference voltage to drive the liquid crystal cells,

8. However, it might be argued that the description of **Kawaguchi** (figure 1A) does not explicitly state that the first and second line-one glass signal pads (or line on glass signal lines) are on respective intersecting sides which define one corner of the outer area of the picture display part, since that description does not explicitly refer to figure 1A of **Kawaguchi**. The examiner believes that one of ordinary skill in the art would understand the reference to be disclosing such a corner in figure 5. Assuming for the sake of argument that **Kawaguchi** does not disclose such a corner, the examiner cites **Yuda et al.** (see at least figure 10), which teaches that the first and second line-one

glass signal pads (or line on glass signal lines) are on respective intersecting sides which define one corner of the outer area of the picture display part (2a) in order to supply the input signal from an external device to the liquid crystal panel and reduce the length of the input signal lines formed on the liquid crystal panel.

9. In other words, **Kawaguchi as modified by Yuda et al.** also teaches a plurality of first dummy pads between the first line-on glass type signal pads and a plurality of second dummy pads between the second line-on glass type signal pads.

10. **Kawaguchi** is silent regarding forming the insulating layer. **Kim et al.** (in at least paragraph 22, figures 1, 3-4, 6) teaches the insulating film covers the plurality of line-on glass type signal lines and the dummy line (700) is formed on the layer of the insulating film (660). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the insulating film as taught by **Kim et al.** because such modification would reduce the EMI effect and the wireless frequency interference.

11. Regarding **claim 5**, **Kim et al.** (figures 1, 3-4, 6) discloses the line-on glass type signal lines (620) are formed in a same layer as the gate line (621) of the picture display part.

12. Regarding **claim 6, Kim et al.** (figures 1, 3-4, 6) discloses the dummy line (700) is formed in a same layer as a data line (621, figure 4) of the picture display part with a gate insulating film therebetween (660).

13. Regarding **claim 12**, **Kawaguchi** (figure 1A) discloses a fabricating method of a line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides (figure 5), comprising:

- forming first ~ n(th) gate lines in a picture display part and a plurality of line-on glass signal lines (13; see at least column 6, lines 60-65) in one comer of an outer area of the picture display part on a substrate for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part (see at least column 4, lines 30-35);
- forming first ~ n(th) data lines (11) to cross the first ~ n(th) gate lines in a picture display part and a dummy line (12) that is located between the line-on glass signal lines for applying a common voltage as a reference voltage; and
- **Kawaguchi** (figure 1A) implicitly discloses forming first ~ n(th) data pads extended from the first ~ n(th) data lines and first ~ n(th) gate pads extended from the first ~ n(th) gate lines on an intersecting side of the outer area of the picture display part and forming first and second line-on glass signal pads just beside the first data pad and the first gate pad, respectively, and first dummy pads between the first line-on glass signal pads and second dummy pads between the second line-on glass pads, respectively, the intersecting sides defining one comer of the outer area of the picture display part;
- wherein each of the plurality of the line-on glass signal lines is connected between the first and the second line-on glass signal pads in the one corner of the outer area of the picture display part.

14. However, it might be argued that the description of **Kawaguchi** (figure 1A) does not explicitly state that the first and second line-one glass signal pads (or line on glass signal lines) are on respective intersecting sides which define one corner of the outer area of the picture display part, since that description does not explicitly refer to figure 1A of **Kawaguchi**. The examiner believes

that one of ordinary skill in the art would understand the reference to be disclosing such a corner in figure 5. Assuming for the sake of argument that **Kawaguchi** does not disclose such a corner, the examiner cites **Yuda et al.** (see at least figure 10), which teaches that liquid crystal display panel having sides and corners defined at intersections of the sides; the first and second line-one glass signal pads (or line on glass signal lines) are on respective intersecting sides which define one corner of the outer area of the picture display part (2a) in order to supply the input signal from an external device to the liquid crystal panel and reduce the length of the input signal lines formed on the liquid crystal panel.

15. In other words, **Kawaguchi as modified by Yuda et al.** also teaches first dummy pads between the first line-on glass signal pads and second dummy pads between the second line-on glass pads, respectively, the intersecting sides defining one comer of the outer area of the picture display part.

16. **Kawaguchi** is silent regarding forming the insulating layer. **Kim et al.** (in at least paragraph 22, figures 1, 3-4, 6) teaches forming at least one layer of insulating film (660) to cover the line-on glass type signal lines (620 or 621) and the dummy line (700) is formed on the layer of the insulating film (see at least paragraph 0039). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the insulating film as taught by **Kim et al.** because such modification would reduce the EMI effect and the wireless frequency interference.

17. Regarding **claim 13**, **Kim et al.** (figures 1, 3-4, 6) discloses forming a gate electrode connected to the gate line of the picture display part on the substrate; forming a gate insulating film (660) on the substrate on which the gate line and the gate electrode are formed; forming a

semiconductor layer on the gate insulating film; forming a source electrode connected to the data line, and a drain electrode opposite to the source electrode with a designated gap therebetween (630), on the substrate on which the semiconductor is formed; forming a protective film (660) on the substrate where the data line, the source electrode and the drain electrode are formed; and forming a pixel electrode (650) connected to the drain electrode on the protective film.

18. Regarding **claim 14**, **Kim et al.** (figures 1, 3-4, 6) discloses the line-on glass signal lines are formed of a same metal as a gate line (62').

19. Regarding **claim 15**, **Kim et al.** (figures 1, 3-4, 6) discloses the dummy line is formed of a same metal as the data line (700 and 621).

20. Regarding **claim 16**, **Kim et al.** (figures 1, 3-4, 6) discloses the dummy line (700) is formed between the line-on glass type signal lines (620) with the gate insulating film therebetween (660).

21. Regarding **claim 24**, **Kim et al.** (figures 1, 3-4, 6) discloses a capacitor is formed between a dummy line and a signal type line (700 and 630) for causing an EMI signal to reduce EMI signal interference (capacitance exists when two metal layers are separated by insulating/dielectric layer).

Please note that the claims are directed to apparatus which must be distinguished over the prior art in term of structure rather than functions [MPEP 2114]. Hence, the functional limitations of " for causing an EMI signal to reduce EMI signal interference " which are narrative in form have not been given any patentable weight. In order to be given patentable weight, a functional recitation must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. See In re Danley, 120 USPQ 528, 531 (CCPA 1959).

22. **Claims 19-20 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kawaguchi** in view of **Kim**; further in view of **Yuda et al. and Song et al. (US 2002/0008794)**.

23. Regarding **claim 19**, **Kawaguchi** (figure 1A) discloses a line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides (figure 5), comprising:

- a picture display part with a matrix of liquid crystal cells having a plurality of gate lines and date lines to cross each other (see at least column 4, lines 10-20)
- **Kawaguchi** (figure 1A) implicitly discloses a gate pad and a data pad to drive the gate lines and data lines, respectively, the gate pad and the data pad are formed in an outer area of the picture display part of a lower substrate;
- a plurality of line-on glass type signal lines (13; see at least column 6, lines 60-65) located in one comer of the outer area of the picture display part of the lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one comer of the outer area of the picture display part is defined by the intersections of two sides of said outer area of the lower substrate and wherein the gate pad is adjacent to one of the sides and the data pad is adjacent to the intersecting side;
- a plurality of common voltage signal lines (12) for applying a common voltage signal and being formed between the line-on glass lines,
- wherein at least one of the plurality of common voltage lines applies the common voltage signal through a dot to a common electrode that is formed on an entire surface of an upper substrate (14).

24. However, it might be argued that the description of **Kawaguchi** (figure 1A) does not explicitly state that the first and second line-one glass signal pads (or line on glass signal lines) are on respective intersecting sides which define one corner of the outer area of the picture display part, since that description does not explicitly refer to figure 1A of **Kawaguchi**. The examiner believes that one of ordinary skill in the art would understand the reference to be disclosing such a corner in figure 5. Assuming for the sake of argument that **Kawaguchi** does not disclose such a corner, the

examiner cites **Yuda et al.** (see at least figure 10), which teaches that liquid crystal display panel having sides and corners defined at intersections of the sides; a plurality of line-on glass type signal lines located in one comer of the outer area of the picture display part of the lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one comer of the outer area of the picture display part is defined by the intersections of two sides of said outer area of the lower substrate and wherein the gate pad is adjacent to one of the sides and the data pad is adjacent to the intersecting side (2a) in order to supply the input signal from an external device to the liquid crystal panel and reduce the length of the input signal lines formed on the liquid crystal panel.

25. In other words, **Kawaguchi as modified by Yuda et al.** also teaches a plurality of common voltage signal lines for applying a common voltage signal and being formed between the line-on glass lines.

26. **Kawaguchi** is silent regarding forming the insulating layer and the silver dot. **Kim et al.** (in at least paragraph 22, figures 1, 3-4, 6) teaches forming an insulating film (660) to cover the line-on glass type signal lines (620 or 621) and common voltage signal lines (700) being formed on the layer of the insulating film (see at least paragraph 0039). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the insulating film as taught by **Kim et al.** because such modification would reduce the EMI effect and the wireless frequency interference.

27. In addition, **Song et al.** (in at least paragraph 0014, figure 4) teaches at least one of the plurality of common voltage lines applies the common voltage signal through a silver(Ag) dot (63) to a common electrode that is formed on an entire surface of an upper substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine

the silver dot as taught by **Song et al.** because such modification would provide an electrical connection with the common electrode of the upper substrate.

28. Regarding **claim 20**, **Kawaguchi** (figure 1A) discloses the line-on glass liquid crystal display panel according to claim 19, wherein the gate signal lines are Vgl, Vcc, Vgh, GOE, GSC, OSP.

29. Regarding **claim 24**, **Kim et al.** (figures 1, 3-4, 6) discloses a plurality of dummy lines and an insulating film covering the plurality of line-on glass type signal lines, wherein the dummy lines are formed on the layer of the insulating film, and wherein a capacitor is formed between a dummy line and a signal type line (700 and 630) for causing an EMI signal to reduce EMI signal interference (capacitance exists when two metal layers are separated by insulating/dielectric layer).

Please note that the claims are directed to apparatus which must be distinguished over the prior art in term of structure rather than functions [MPEP 2114]. Hence, the functional limitations of " for causing an EMI signal to reduce EMI signal interference " which are narrative in form have not been given any patentable weight. In order to be given patentable weight, a functional recitation must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. See In re Danley, 120 USPQ 528, 531 (CCPA 1959).

30. **Claims 21-22 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kawaguchi** in view of **Yuda et al.**.

31. Regarding **claim 21**, **Kawaguchi** (figure 1A) discloses a line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides (figure 5), comprising:

- a picture display part with a matrix of liquid crystal cells having a plurality of gate lines and date lines to cross each other (see at least column 4, lines 10-20)
- **Kawaguchi** (figure 1A) implicitly discloses a gate pad and a data pad to drive the gate lines and data lines, respectively, the gate pad and the data pad are formed in an outer area of the

picture display part of a lower substrate on respective intersecting sides which define one corner;

- a plurality of line-on glass type signal lines (13; see at least column 6, lines 60-65) located in one comer of the outer area of the picture display part of the lower substrate extending from one side to the other intersecting side that defines the one corner for applying drive signals to drive the liquid crystal cells, wherein the plurality of line-on glass signal lines are between the gate pad and the data pad; and
- a common voltage line (12) located in the one corner, wherein the common voltage line is adjacent to both the gate pad and the data pad (according to figure 4 of the instant application, the common voltage line 52 is most adjacent to the pads while having other pads/ lines in between. Therefore, the common voltage line as disclosed by **Kawaguchi** is also adjacent to both the pads).

32. However, it might be argued that the description of **Kawaguchi** (figure 1A) does not explicitly state that the first and second line-one glass signal pads (or line on glass signal lines) are on respective intersecting sides which define one corner of the outer area of the picture display part, since that description does not explicitly refer to figure 1A of **Kawaguchi**. The examiner believes that one of ordinary skill in the art would understand the reference to be disclosing such a corner in figure 5. Assuming for the sake of argument that **Kawaguchi** does not disclose such a corner, the examiner cites **Yuda et al.** (see at least figure 10), which teaches that liquid crystal display panel having sides and corners defined at intersections of the sides; a plurality of line-on glass type signal lines located in one comer of the outer area of the picture display part of the lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one comer of the outer area of

the picture display part is defined by the intersections of two sides of said outer area of the lower substrate and wherein the gate pad is adjacent to one of the sides and the data pad is adjacent to the intersecting side (2a) in order to supply the input signal from an external device to the liquid crystal panel and reduce the length of the input signal lines formed on the liquid crystal panel.

33. In other words, **Kawaguchi as modified by Yuda et al.** also teaches a plurality of common voltage signal lines for applying a common voltage signal and being formed between the line-on glass lines.

34. Regarding **claim 22**, **Kawaguchi** (figure 1A) discloses the gate signal lines are Vgl, Vet, Vgh, GOE, GSC, GSP.

35. Regarding **claim 24**, **Kim et al.** (figures 1, 3-4, 6) discloses a plurality of dummy lines and an insulating film covering the plurality of line-on glass type signal lines, wherein the dummy lines are formed on the layer of the insulating film, and wherein a capacitor is formed between a dummy line and a signal type line (700 and 630) for causing an EMI signal to reduce EMI signal interference (capacitance exists when two metal layers are separated by insulating/dielectric layer).

Please note that the claims are directed to apparatus which must be distinguished over the prior art in term of structure rather than functions [MPEP 2114]. Hence, the functional limitations of " for causing an EMI signal to reduce EMI signal interference " which are narrative in form have not been given any patentable weight. In order to be given patentable weight, a functional recitation must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. See In re Danley, 120 USPQ 528, 531 (CCPA 1959).

36. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kawaguchi** in view of **Yuda et al. and Song et al. (US 2002/0008794)**.

37. Regarding **claim 23**, **Kawaguchi** discloses the limitations as shown in the rejection of **claim 21** above. However, **Kawaguchi** is silent regarding forming the silver dot. **Song et al.** (in at least paragraph 0014, figure 4) teaches the common voltage lines applies the common voltage

signal through a silver(Ag) dot (63) to a common electrode that is formed on an entire surface of an upper substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the silver dot as taught by **Song et al.** because such modification would provide an electrical connection with the common electrode of the upper substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lauren Nguyen whose telephone number is (571) 270-1428. The examiner can normally be reached on M-Th, 7:30-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lauren Nguyen/
Examiner, Art Unit 2871